


Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete if Known	
Application Number		10/083,241			
Filing Date		February 25, 2002			
First Named Inventor		Yervant Zorian			
Art Unit		2133			
Examiner Name		Ton, David			
Attorney Docket Number		4640P006			
Sheet	1	of	2		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No.¹	Document Number	Publication Date or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code² (if known)			
DT		US-6,181,614	01-30-2001	Aipperspach et al.	
		US-6,304,989	10-16-2001	Kraus et al.	
		US-6,408,401	06-18-2002	Bhavsar et al.	
		US-6,067,262	05-23-2000	Irrinki et al.	
		US-5,583,463	12-10-1996	Merritt	
		US-5,608,678	03-04-1997	Lysinger	
		US-6,396,760	05-28-2002	Behera et al.	
		US-6,519,202	02-11-2003	Shubat et al.	
		US-6,795,942	09-21-2004	Schwarz et al.	
		US-6,691,252	02-10-2004	Hughes et al.	
DT		US-6,574,757	06-03-2003	Park et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T
		Country Code³ - Number⁴ - Kind Code⁵ (if known)				

Examiner Signature		Date Considered	11/20/2005
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. *Applicant is to place a check mark here if English language Translation is attached.

Based on PTO/SB/08A (08-03) as modified by Blakely, Solakoff, Taylor & Zafman (wr) 08/11/2003.

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Substitute for form 43A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Complete if Known	
				Application Number	10/083,241
Sheet 2 of 2				Filing Date	February 25, 2002
				First Named Inventor	Yervant Zorian
				Art Unit	2133
				Examiner Name	Ton, David
				Attorney Docket Number	4640P006

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.†	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T†
DT		TSIN-YUANCHANG et al., "Tutorial 2: SoC Testing and P1500 Standard", Asian Test Symposium 2000: 492	
		ERIK JAN MARINISSEN et al., "Wrapper Design for Embedded Core Test", ITC 2000: 911-920.	
		ALFREDO BENSO et al., "HD-BIST: A Hierarchical Framework for BIST Scheduling and Diagnosis in SOCS", ITC 1999: 1038-1044	
		D. GIZOPOULOS et al., "Low Power/Energy BIST Scheme for Datapaths", VTS 2000: pp. 6 total.	
		V.A. VARDANIAN et al., "A March-based Fault Location Algorithm for Static Random Access Memories", MDTD 2002: 256-261 July 10-12, 2002	
		ALFREDO BENSO et al., "HD2BIST: a Hierarchical Framework for BIST Scheduling, Data patterns delivering and diagnosis in SoCs", ITC 2000: pp. 10 total.	
		YERVANT ZORIAN et al., "Embedded-Memory Test and Repair: Infrastructure IP for SoC Yield", IEEE CS and IEEE CASS May-June 2003: 58-66	
		YERVANT ZORIAN et al., "Embedding Infrastructure IP for SoC Yield Improvement", June 2002, pp. 709-712.	
DT		PRAVEEN PARVATHALA et al., "FRITS-A Microprocessor Functional BIST Method", March 2002, pp. 590-598	

Examiner Signature	<i>David Ton</i>	Date Considered	11/20/2005
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